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Logic Design Lab Viva Questions

Digital Logic Design VIVA Questions :- 1) Explain about setup time and hold time, what will happen if there is setup time and hold time violation, how to overcome this? Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.

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Logic Design Laboratory Manual 3 ____ VIVA QUESTIONS: 1. Why NAND & NOR gates are called universal gates? 2. Realize the EX – OR gates using minimum number of NAND gates. 3. Give the truth table for EX-NOR and realize using NAND gates? 4. What are the logic low and High levels of TTL IC's and CMOS IC's? 5. Compare TTL logic family with ...

LOGIC DESIGN LABORATORY MANUAL - ElectricVLab

250+ Digital Logic Design Interview Questions and Answers. Question1: Explain about setup time and hold time, what will happen if there is setup time and hold time violation, how to overcome this? Question2: What is skew, what are problems associated with it and how to minimize it? Question3: What is slack? Question4: What is glitch? What causes it (explain with waveform)?

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Digital Electronics Viva Question With Answer

Switching Theory and Logic Design UNIT WISE important Questions and Answers :-UNIT-III. 1. Design of halfadder, half subtractor by using basic gates and universal gates with necessary expressions. 2. Design fulladder& full subtractor by using universal gates and using two half sub tractors basic half adders with necessary Boolean functions. 3.

50 TOP Switching Theory and Logic Design UNIT WISE ...

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Define combinational logic When logic gates are connected together to produce a specified output for certain specifiedcombinations of input variables, with no storage involved, the resulting circuit is calledcombinational logic.64. Explain the design procedure for combinational circuits € The problem definition € The determination of number ...

Digital logic circuits important question and answers for ...

VLSI Lab viva question with answersSynchronous reset logic will synthesize to smaller flip-flops, particularly if the reset is gated withthe logic generating the d-input. But in such a case, the combinational logic gate count grows, sothe overall gate count savings may not be that significant.

Visi lab viva question with answers - SlideShare

For a state machine with 9- 16 states, a binary FSM only requires 4 flip-flops while a one hot FSM requires a flip-flop for each state in the design FPGA vendors frequently recommend using a one hot state encoding style because flip-flops are plentiful in an FPGA and the combinational logic required to implement a one hot FSM design is typically smaller than most binary encoding styles.

Interview and viva questions and answers on Digital ...

Last Minute Notes (LMNs) Quizzes on Digital Electronics and Logic Design; Practice Problems on Digital Electronics and Logic Design ! Please write comments if you find anything incorrect, or you want to share more information about the topic discussed above.

Digital Electronics and Logic Design Tutorials - GeeksforGeeks

It has two inputs A and B and two outputs S (sum) and C (carry). It is represented by XOR logic gate and an AND logic gate. Truth Table of Half adder: 25) What is Full-Adder? Full-adder is the circuits that perform the addition of three bits. It has three inputs A, B and a carry bit. Full adders are represented with AND, OR and XOR logic gate.

Top 39 Digital Electronics Interview Questions - Javatpoint

Microcontroller and microprocessors lab viva questions with answers, MPMC Lab viva questions, Microprocessors and Interfacing Lab viva questions with answers, MPI lab viva questions.MPMC Lab 1.What is a Microprocessor? It is a CPU fabricated on a single chip, program-controlled device, which fetches the instructions from memory, decodes and executes the instructions.

Microprocessors and Microcontroller Lab viva Questions ...

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Fluid Mechanics Viva Questions Answers

draw full subtractor circuit by using half subtractor circuit and digital electronics lab viva questions ... on a control signal viva questions 47 48 7 appendix 1 49 52 2 full adder using basic logic gates b full subtractor is a logical circuit which performs subtraction of three bits and provides an output with a

Viva Questions Of Full Adder And Subtractor In Dsd Lab

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